DERWENT-ACC-NO: 2001-661021

DERWENT-WEEK: 200176

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TITLE: Eisc processor

INVENTOR: SONG, J H

PATENT-ASSIGNEE: LG ELECTRONICS INC[GLDS]

PRIORITY-DATA: 1999KR-0060180 (December 22, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES
MAIN-IPC			
KR 2001063191 A	July 9, 2001	N/A	001
G06F 001/00			

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001063191A	N/A	1999KR-0060180	December 22, 1999

INT-CL (IPC): G06F001/00

ABSTRACTED-PUB-NO: KR2001063191A

BASIC-ABSTRACT:

NOVELTY - An EISC processor is provided to perform a plurality of instruction languages which cannot fetch at one time in one cycle by making the instructions as one instruction language.

DETAILED DESCRIPTION - An instruction language buffer(200) receives instruction languages from a cache memory(100) by one cycle and stores the instruction languages successively. A folding unit(300) checks the instruction languages stored in the instruction language buffer(200) in accordance with a stored order and detects a combination of a proper instruction. A decoding unit(400) receives an output signal of the folding unit(300) and decodes the signal and outputs an instruction in accordance with the signal. A register(500) reads data having a predetermined address by an instruction language of the decoding unit(400). An executing unit(600) executes the instruction by reading the data having a predetermined address of the register(500) and stores the executing data in the register(500). The cache memory(100) stores the instruction language.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: PROCESSOR

DERWENT-CLASS: T01

EPI-CODES: T01-X;

DERWENT-ACC-NO: 2004-007199

DERWENT-WEEK: 200401

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TITLE: Device and method for folding instruction of eisc processor

INVENTOR: LEE, J I; SONG, S C

PATENT-ASSIGNEE: LG ELECTRONICS INC[GLDS]

PRIORITY-DATA: 2002KR-0007506 (February 8, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2003067364 A	August 14, 2003	N/A	001	G06F 009/30

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2003067364A	N/A	2002KR-0007506	February 8, 2002

INT-CL (IPC): G06F009/30

ABSTRACTED-PUB-NO: KR2003067364A

BASIC-ABSTRACT:

NOVELTY - A device and a method for folding an instruction of an EISC(Extendable Instruction Set Computer) processor are provided to reduce a cycle number of the processor due to an Leri(Load extension register immediate) instruction used for extending the instruction, and to remove the waste time and the fall of the processor performance by using an instruction queue.

DETAILED DESCRIPTION - An instruction memory(11) simultaneously outputs a constant number of instructions stored in an address and the sequential addresses. A Leri decoder(13) distinguishes the Leri information by reading and decoding the instructions from the instruction memory(11). A crossbar switch(12) inputs the instructions from the instruction memory(11) at one time, receives the Leri instruction existence from the Leri decoder(13), and selectively switches and outputs the instructions according to the Leri instruction existence of the highest instruction. A decoder(14) decodes a non-Leri instruction from the crossbar switch(12) if the highest instruction is the Leri instruction, and decodes the highest instruction.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: DEVICE METHOD FOLD INSTRUCTION PROCESSOR

DERWENT-CLASS: T01

EPI-CODES: T01-F03;

DERWENT-ACC-NO: 2004-007200

DERWENT-WEEK: 200401

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TITLE: Device and method for folding instruction of eisc processor

INVENTOR: LEE, J I; SONG, S C

PATENT-ASSIGNEE: LG ELECTRONICS INC[GLDS]

PRIORITY-DATA: 2002KR-0007507 (February 8, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2003067365 A	August 14, 2003	N/A	001	G06F 009/30

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2003067365A	N/A	2002KR-0007507	February 8, 2002

INT-CL (IPC): G06F009/30

ABSTRACTED-PUB-NO: KR2003067365A

BASIC-ABSTRACT:

NOVELTY - A device and a method for folding an instruction of an EISC(Extendable Instruction Set Computer) processor are provided to reduce the power consumption by preventing the unnecessary connection of an instruction memory and to reduce the complexity of design using a simple program counter.

DETAILED DESCRIPTION - An instruction memory(11) simultaneously outputs a constant number of instructions stored in an address and the sequential addresses. A Leri decoder(13) distinguishes the Leri information by decoding the instructions fetched from the instruction memory(11). The program counter(17) outputs the address of the next executing instruction from the instruction memory(11), checks a number of the non-Leri instruction from the Leri decoder(13), and stops increasing address of the instruction memory(11) during an instruction executing cycle of the fetched instructions. A crossbar switch(12) inputs the instructions fetched from the instruction memory(11) at one time, receives the Leri instruction existence from the Leri decoder(13), and selectively switches and outputs the instructions according to the Leri instruction existence of the highest instruction.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: DEVICE METHOD FOLD INSTRUCTION PROCESSOR

DERWENT-CLASS: T01

EPI-CODES: T01-F03;